LMZ20502 2A SIMPLE SWITCHER ® Nano Module

Check for Samples: LMZ20502

FEATURES

- **Integrated inductor**
- **Miniature 3.5mm x 3.5mm x 1.7mm package**
- **-40°C to 125°C junction temperature range**
- **Power good flag function**
- **Pin selectable switching modes**
- **Adjustable output voltage**
- **3.0MHz Fixed PWM Switching Frequency**
- **Internal compensation and soft-start**
- **Current limit, thermal shutdown, and UVLO protection**
- **Requires only 5 external components**

ELECTRICAL SPECIFICATIONS

- **2A maximum load current**
- **Input voltage range 2.7V to 5.5V**
- **Output voltage range 0.8V to 3.6V**
- **± 1% feedback tolerance over temperature**
- **1 µA (max) quiescent current in shutdown**
- **64 µA (typ) quiescent current**

PERFORMANCE BENEFITS

- **Small solution size**
- **Easy component selection and simple PCB layout**
- **High efficiency reduces system heat generation**

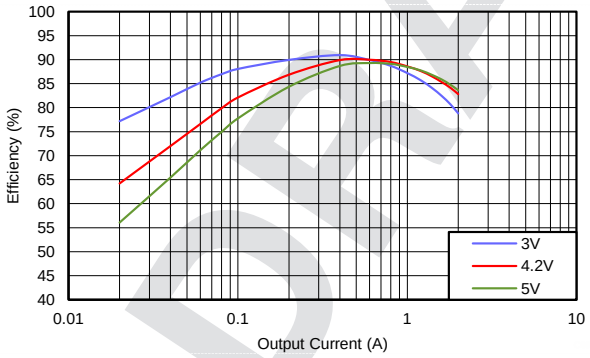

Figure 1. Typical Efficiency for V_{OUT} = 1.8V AUTO MODE

DESCRIPTION

The LMZ20502 SIMPLE SWITCHER ® Nano Module regulator is an easy to use synchronous step-down DC-DC converter capable of driving up to 2A of load from an input of up to 5.5V, with exceptional efficiency and output accuracy in a very small solution size. The innovative package contains the regulator and inductor in a small 3.5mm x 3.5mm x 1.7mm volume. Thus saving board space and eliminating the time and expense of inductor selection. The LMZ20502 requires few external components and has a pin-out designed for simple, optimum PCB layout. The LMZ20502 is a member of Texas Instruments' SIMPLE SWITCHER ® family. The SIMPLE SWITCHER ® concept provides for an easy to use complete design with a minimum number of external components and the TI WEBENCH ® design tool. TI's WEBENCH ® tool includes features such as external component calculation, electrical simulation, WebTherm ®, and Build-It boards for easy design-in. For soldering information, please refer to the following document: http://www.ti.com/lit/an/snoa401r/snoa401r.pdf

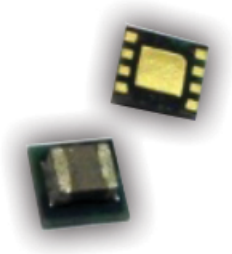

Figure 2. 8 Pin DFN 3.5mm x 3.5mm x 1.7mm 0.8mm Pitch

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Typical Application Circuit

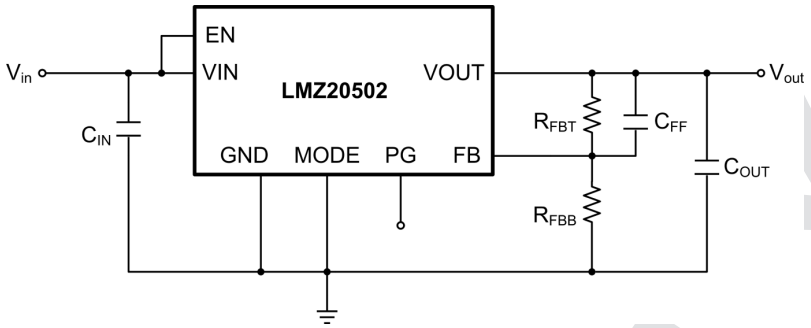
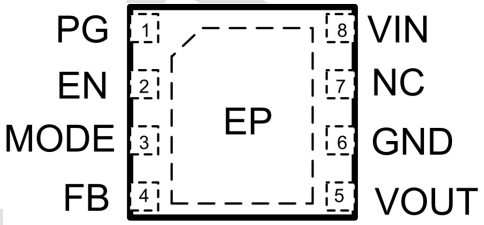


Figure 3. Typical Application Circuit
See Table 1

Table 1. RECOMMENDED COMPONENT VALUES

VOUT	R_{FBB}	R_{FBT}	COUT	C_{FF}	CIN
0.8V	121 kΩ	40.2 kΩ	2x 10µF	39 pF	2x 10µF
1.2V	30.1 kΩ	30.1 kΩ	10 µF	20 pF	2x 10µF
1.8V	40.2 kΩ	80.6 kΩ	10 µF	16 pF	2x 10µF
2.5V	47.5 kΩ	150 kΩ	10 µF	12 pF	2x 10µF
3.3V	53.2 kΩ	237 kΩ	10 µF	82 pF	2x 10µF
3.6V	53.2 kΩ	267 kΩ	10 µF	82 pF	2x 10µF

Connection Diagram



TOP VIEW

Figure 4. Connection Diagram

PIN DESCRIPTIONS

Pin #	NAME	TYPE (1)	Description
1	PG	O	Power good flag; open drain. Connect to logic supply through a resistor. High = power good; Low = power bad
2	EN	I	Enable input. High = On, Low = Off. A valid input voltage must be present before EN is asserted. Do not float
3	MODE	I	Mode selection input. HIgh = forced PWM. Low = auto mode, with PFM at light load . Do not float.
4	FB	I	Feedback input to controller. Connect to output through feedback divider.
5	VOUT	P	Regulated output voltage.
6	GND	G	Ground for all circuitry. Reference point for all voltages.
7	NC		This pin must be left floating. Do not connect to ground.

(1) G = Ground, I = Input, O = Output, P = Power

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PIN DESCRIPTIONS (continued)

Pin #	NAME	TYPE(1)	Description
8	VIN	P	Input supply to regulator. Connect a bypass capacitor as close as possible to the VIN pin and GND pin of the module
EP	EP	G	Ground and heatsink connection.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

	VALUE		UNIT
	MIN	MAX	
VIN to GND	-0.2	6	V
EN, MODE, FB, PG, to GND(2)	-0.2	VIN+0.2	V
VOUT to GND(2)	-0.2	VIN+0.2	V
Junction Temperature		150°	C
Storage Temperature	-65°	150°	C
ESD Susceptibility(3)	-2	2	kV
Peak Soldering Reflow Temperature for Pb(4)		240°	C
Peak Soldering Reflow Temperature for No-Pb(4)		260°	C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see Electrical Characteristics.
(2) The absolute maximum voltage on this pin must not exceed 6V with respect to ground.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.
(4) For soldering information, please refer to the following document: http://www.ti.com/lit/an/snoa401r/snoa401r.pdf

Recommended Operating Conditions(1)

	MIN	MAX	UNIT
Input Voltage Range	2.7	5.5	V
Output Voltage Range(2)	0.8	3.6	V
Load Current Range	0	2	A
Power Good Flag Current	0	4	mA
Junction Temperature	-40°	125°	C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see Electrical Characteristics
(2) Under no conditions should the output voltage be allowed to fall below zero volts.

Thermal Properties(1)

		TYP	UNIT
θ_{JA}	Thermal impedance from junction to ambient	51	°C/W

(1) Taken on a four layer board with a copper area of 9 cm^2 on each layer. Two ounce copper on top and bottom layers and one ounce copper on inner layers, 0.5W power dissipation and no air flow.

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Electrical Characteristics

Limits apply over the recommended operating junction temperature range of -40°C to 125°C, unless otherwise noted. Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_j=25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 3.6V

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
V_{FB}	Feedback Voltage	V_{IN} = 3.6V	0.594	0.6	0.606	V
I_{Q_auto}	Operating quiescent current in Auto mode	Auto Mode		64	80	µA
I_{Q_PWM}	Operating quiescent current in PWM mode	PWM Mode		490	600	µA
I_{Q_off}	Shutdown quiescent current	V_{IN} = 5.5V, V_{EN} = 0.0V(2)		0.03	1	µA
V_{UVLO}	Input supply under voltage lock-out thresholds	Rising		2.5		V
		Falling		2.3		
V_{EN}	Enable input thresholds	V_{IH}	1.2			V
		V_{IL}			0.4	
V_{MODE}	Mode input thresholds	V_{IH}	1.2			V
		V_{IL}			0.4	
I_{LIM}	Peak switch current limit(3)		2.3	2.6		A
F_{osc}	Internal oscillator frequency		2.7	3.0	3.3	MHz
T_{ON}	Minimum switch on-time			50		ns
T_{ss}	Soft start time			800		µs
R_{PG}	Power good flag pull-down R_{dson}		62		76	Ω
V_{PG1}	Power good flag, under-voltage trip(4)	% of feedback voltage, rising		92		%
V_{PG2}	Power good flag, under-voltage trip(4)	% of feedback voltage, falling		88		%
V_{PG3}	Power good flag, over-voltage trip(4)	% of feedback voltage, rising		112		%
V_{PG4}	Power good flag, over-voltage trip(4)	% of feedback voltage, falling		108		%
T_{SD}	Thermal shutdown	Rising Threshold		159		°C
	Thermal shutdown hysteresis			15		°C

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Shutdown current includes leakage current of the switching transistors.
(3) This is the peak switch current limit measured with a slow current ramp. Due to inherent delays in the current limit comparator, the peak current limit measured at 3MHz will be larger.
(4) See Power Good Flag Function for explanation of voltage levels.

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System Characteristics

The following specifications apply to the typical application circuit and the components found in Table 3. **These parameters are not guaranteed and represent typical performance only.** Unless otherwise stated the following conditions apply: T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Load Regulation	Percent output voltage change for the given load current change	V_{OUT} =1.2V, V_{IN}=5V, I_{OUT}=0A to 2A, PWM		0.4		%
		V_{OUT} =1.8V V_{IN}=5V, I_{OUT}=0A to 2A, PWM		0.4		
		V_{OUT} =3.3V V_{IN}=5V, I_{OUT}=0A to 2A, PWM		0.2		
Line Regulation	Percent output voltage change for the given change in input voltage	V_{OUT} = 1.2V I_{OUT}=2A, V_{IN}=3V to 5V, PWM		0.2		%
		V_{OUT} = 1.8V I_{OUT}=2A, V_{IN}=3V to 5V, PWM		0.15		
		V_{OUT} = 3.3V I_{OUT}=2A,V_{IN}=4V to 5V, PWM		0.18		
$V_{R\text{-}PWM}$	Output voltage ripple in PWM	V_{OUT} = 1.2V I_{OUT}=1A, V_{IN}=5V, PWM		3.3		mV pk-pk
		V_{OUT} = 1.8V I_{OUT}=1A,V_{IN}=5V, PWM		3.3		
		V_{OUT} = 3.3V I_{OUT}=1A,V_{IN}=5V, PWM		4.2		
$V_{R\text{-}PFM}$	Output voltage ripple in PFM	V_{OUT} = 1.2V I_{OUT}=1mA, V_{IN}=3V, PFM		22		mV
		V_{OUT} = 1.8V I_{OUT}=1mA, V_{IN}=3V, PFM		22		
		V_{OUT} = 3.3V I_{OUT}=1mA,V_{IN}=5V, PFM		40		
Load Transient	Output voltage deviation from nominal due to a load current step	Vout=1.2V V_{IN}=5V, I_{OUT} = 0A to 2A, Tr=Tf=2µs, PWM		+/- 115		mV
		Vout=1.8V V_{IN}=5V, I_{OUT} = 0A to 2A, Tr=Tf=2µs, PWM		+/- 100		
		Vout=3.3V V_{IN}=5V, I_{OUT} = 0A to 2A, Tr=Tf=2µs, PWM		+/- 150		
Line Transient	Output voltage deviation due to an input voltage step	Vout=1.2V I_{OUT}=1A, V_{IN}=3V to 5V, Tr=Tf=50µs, PWM		25		mV pk-pk
		Vout=1.8V I_{OUT}=1A, V_{IN}=3V to 5V, Tr=Tf=50µs, PWM		30		
		Vout=3.3V I_{OUT}=1A, V_{IN}=4V to 5V, Tr=Tf=50µs, PWM		20		
η	Peak Efficiency	V_{OUT}=1.2V V_{IN}=3V		87		%
		V_{OUT}=1.8V V_{IN}=3V		91		
		V_{OUT}=3.3V V_{IN}=4.2V		94		
	Full Load Efficiency	V_{OUT}=1.2V V_{IN}=3V, I_{OUT}=2A		74		
		V_{OUT}=1.8V V_{IN}=3V, I_{OUT}=2A		79		
		V_{OUT}=3.3V V_{IN}=4.2V, I_{OUT}=2A		89		

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Typical Performance Characteristics

The following specifications apply to the typical application circuit and the components found in Table 3. Unless otherwise stated the following conditions apply: T_A = 25°C

Efficiency V_{OUT} = 1.8V

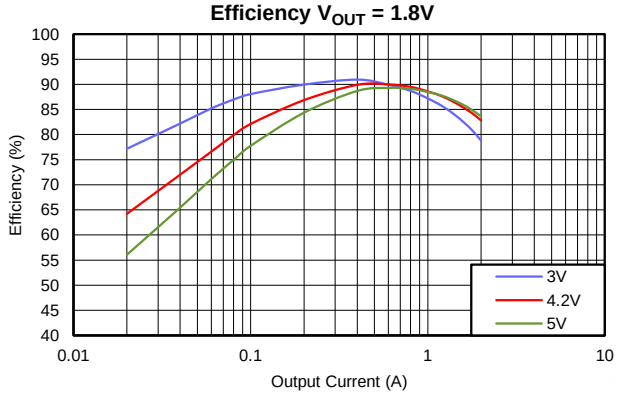

Figure 5.

Load Transient in PWM V_{OUT} = 1.8V, V_{IN} = 4.2V

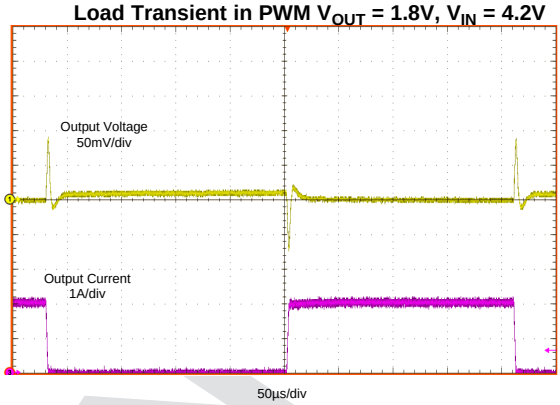

Figure 6.

Regulation V_{OUT} = 1.8V, AUTO Mode

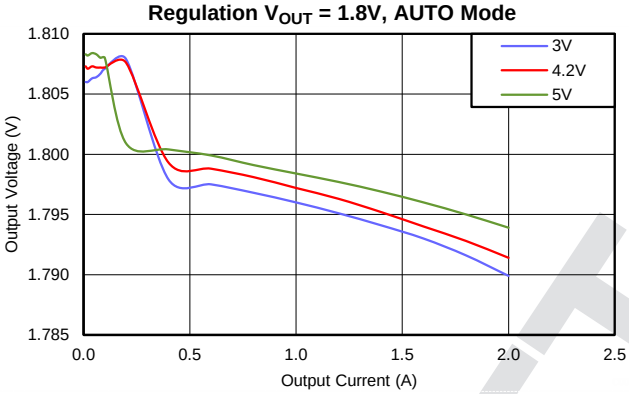

Figure 7.

Load Transient in AUTO Mode V_{OUT} =1.8V, V_{IN} = 4.2V

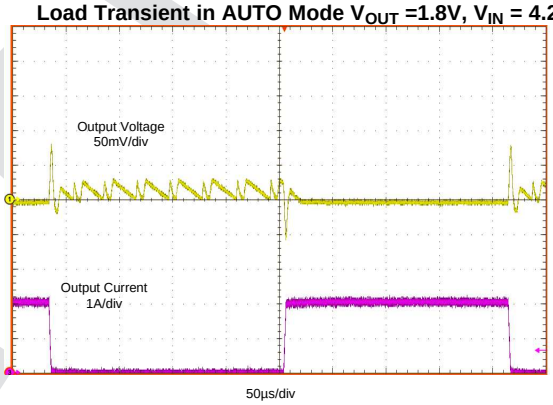

Figure 8.

Auto Mode Thresholds V_{OUT} = 1.8V

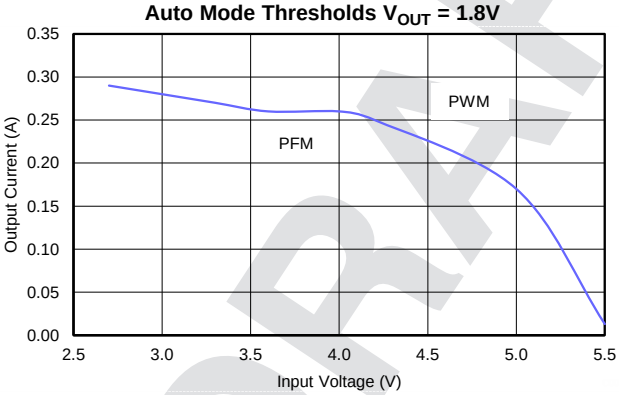

Figure 9.

Start-up V_{OUT} = 1.8V, V_{IN} = 5V, I_{OUT} = 1A

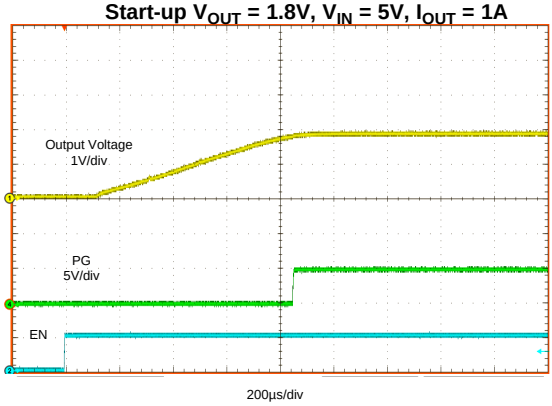

Figure 10.

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Typical Performance Characteristics (continued)

The following specifications apply to the typical application circuit and the components found in Table 3. Unless otherwise stated the following conditions apply: T_A = 25°C

Efficiency V_{OUT} = 1.2V

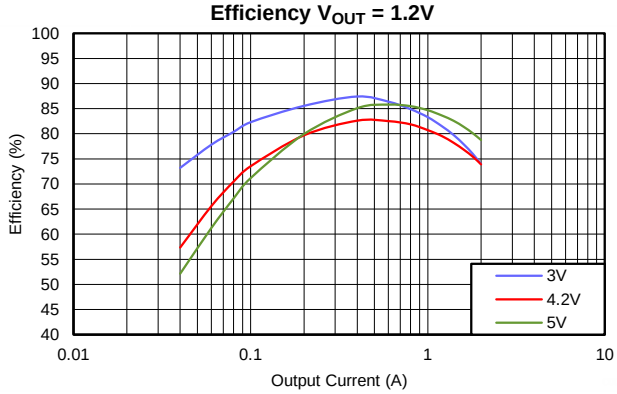

Figure 11.

Load Transients in PWM V_{OUT} = 1.2V, V_{IN} = 4.2V

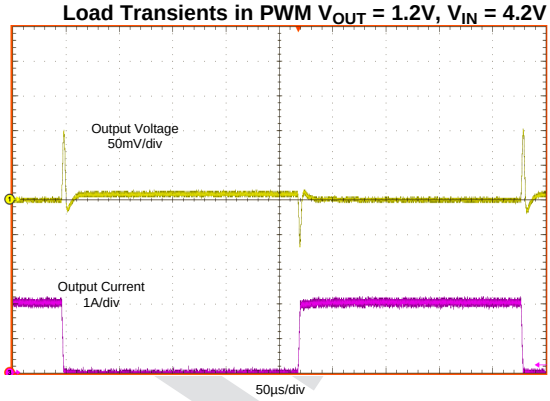

Figure 12.

Regulation V_{OUT} = 1.2V, AUTO Mode

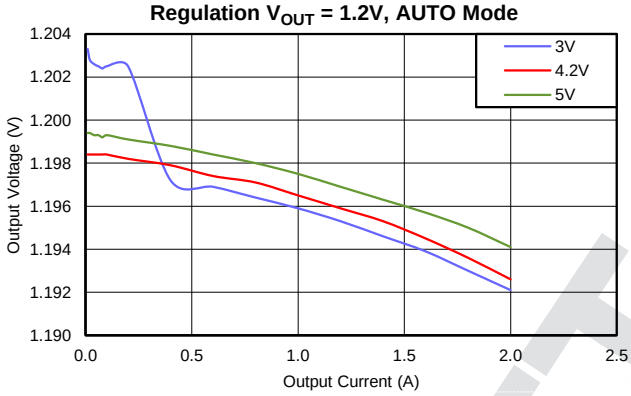

Figure 13.

Load Transients in Auto Mode V_{OUT} = 1.2V, V_{IN} = 4.2V

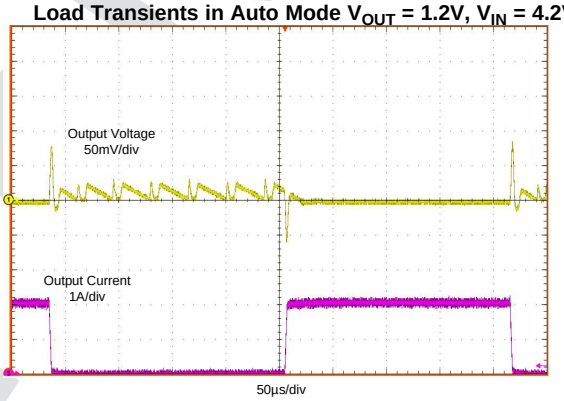

Figure 14.

Auto Mode Thresholds V_{OUT} = 1.2V

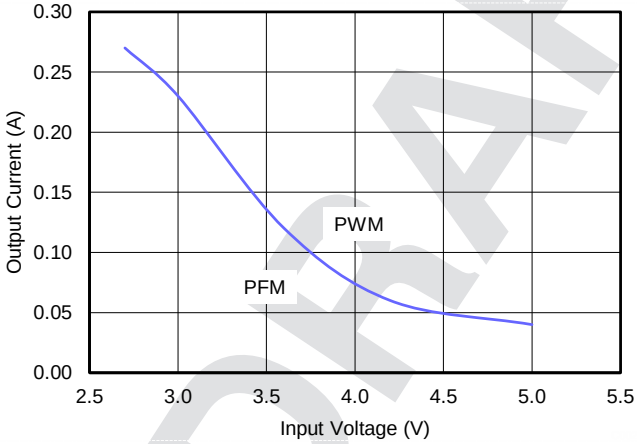

Figure 15.

Start-up V_{OUT} = 1.2V, V_{IN} = 5V, I_{OUT} = 1A

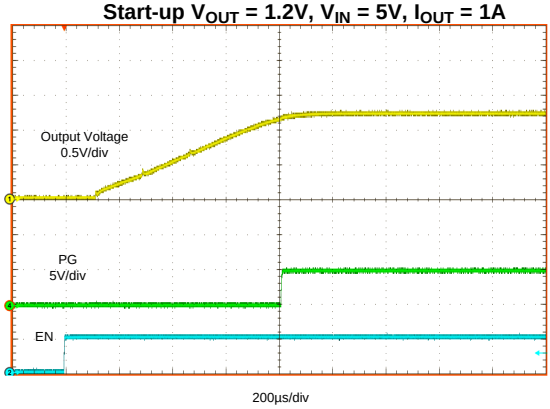

Figure 16.

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Typical Performance Characteristics (continued)

The following specifications apply to the typical application circuit and the components found in Table 3. Unless otherwise stated the following conditions apply: T_A = 25°C

Efficiency V_{OUT} = 3.3V

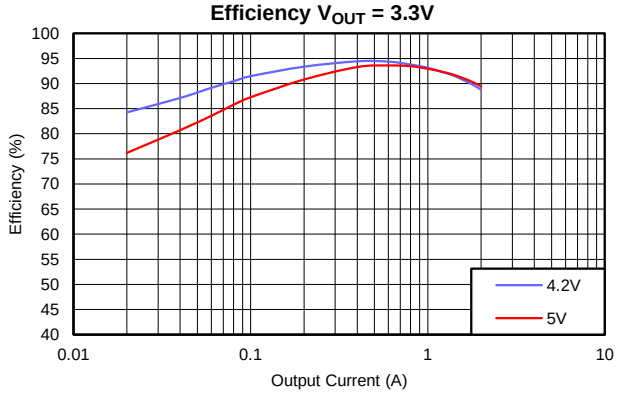

Figure 17.

Load Transients in PWM Mode V_{OUT} = 3.3V, V_{IN} = 5V

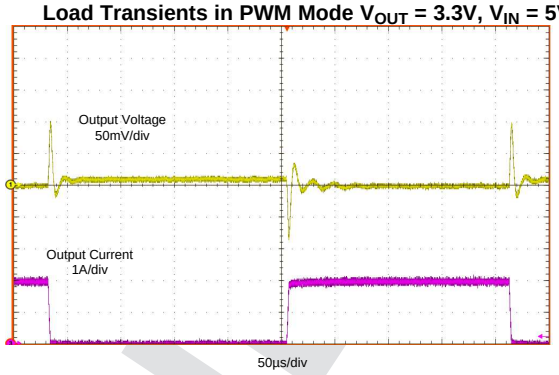

Figure 18.

Regulation V_{OUT} = 3.3V, AUTO Mode

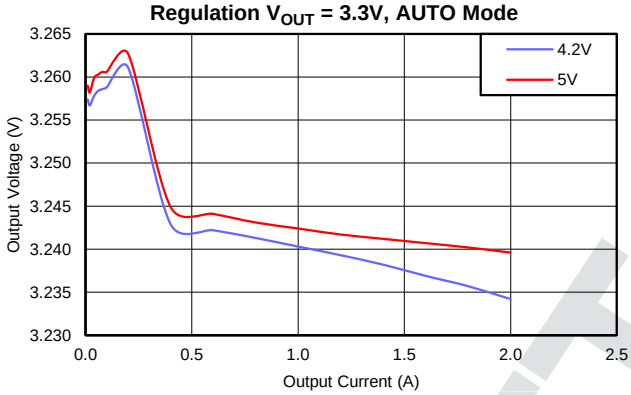

Figure 19.

Load Transients in Auto Mode V_{OUT} = 3.3V, V_{IN} = 5V

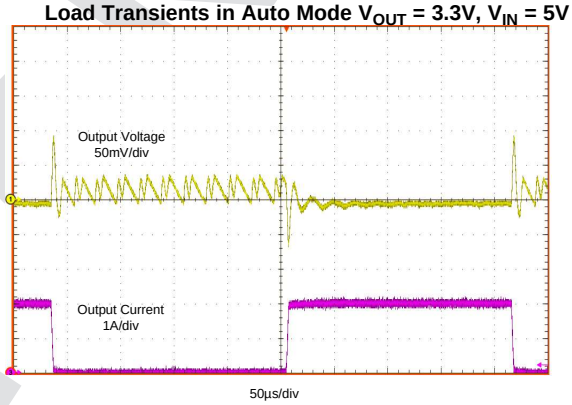

Figure 20.

Auto Mode Thresholds V_{OUT} = 3.3V

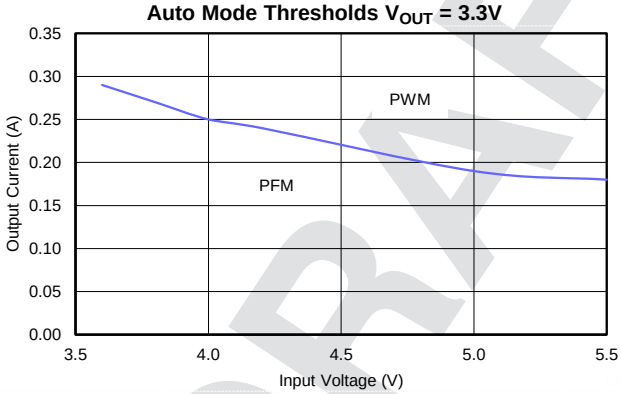

Figure 21.

Start-up V_{OUT} = 3.3V, V_{IN} = 5V, I_{OUT} = 1A

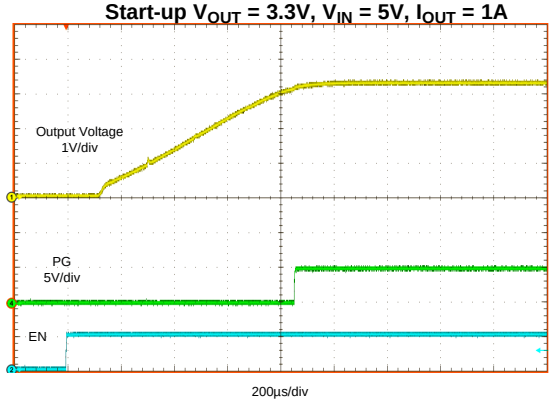

Figure 22.

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Block Diagram

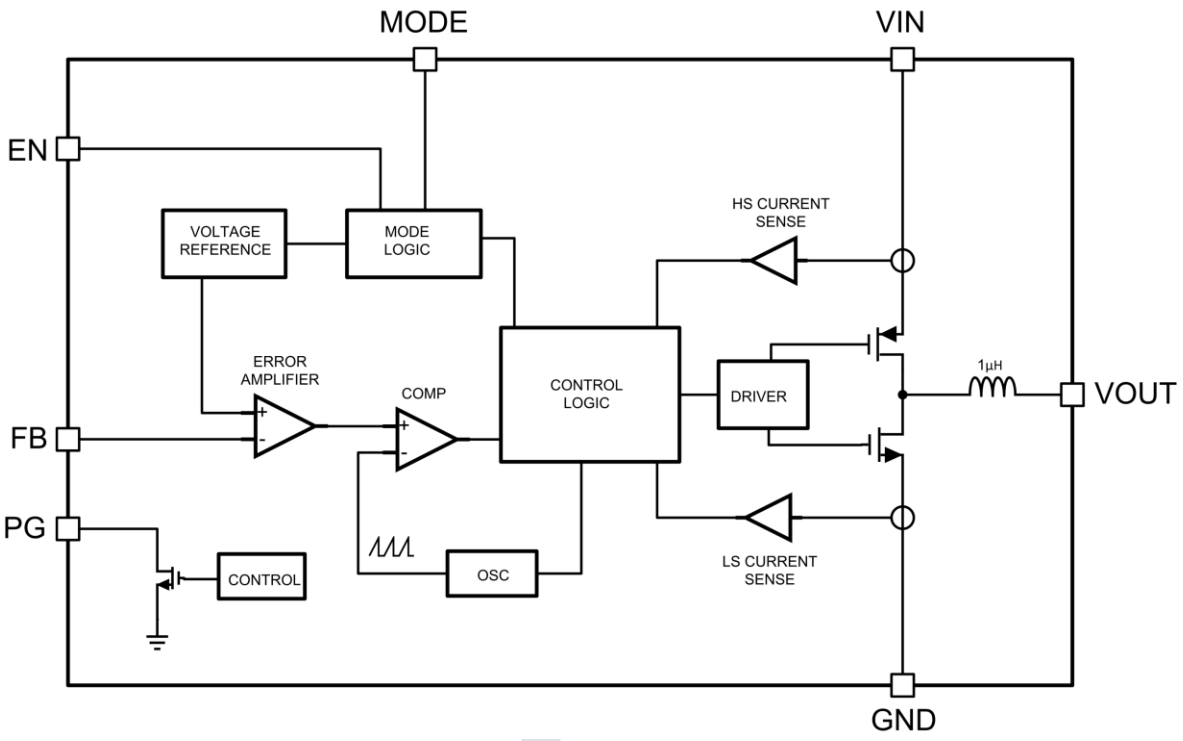

Figure 23. Functional Block Diagram

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OVERVIEW

The LMZ20502 SIMPLE SWITCHER® Nano Module is a voltage mode buck regulator with an integrated inductor. Two operating modes allow the user to tailor the regulator to their specific requirements. In forced PWM mode, the regulator operates as a full synchronous device with a 3.0 MHz (typ.) switching frequency and very low output voltage ripple. This operation is maintained, even at no-load, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple and constant switching frequency. In AUTO mode, the regulator moves into PFM when the load current drops below the mode change threshold (see Typical Performance Characteristics). In PFM, the device regulates the output voltage between wider ripple limits than in PWM. This results in much smaller supply current than in PWM, at light loads. This mode trades off very good light load efficiency for larger output voltage ripple and variable switching frequency.Table 2 describes the mode settings.

Table 2. MODE SELECTION

MODE PIN VOLTAGE	OPERATION
> 1.2V (min)	Forced PWM: The regulator operates in constant frequency, PWM mode for all loads from 0A to full load; no diode emulation is used.
< 0.4V (max)	AUTO Mode: The regulator operates in constant frequency mode for loads greater than the mode change threshold. For loads less than the mode change threshold, the regulator operates in PFM with diode emulation.

PWM Operation

In PWM mode, the converter operates as a voltage mode regulator with input voltage feed-forward. This provides excellent line and load regulation and low output voltage ripple. While in PWM mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load.

PFM Operation

When in AUTO mode, and at light loads, the device enters PFM. The regulator estimates the load current by measuring both the high side and low side switch currents. This estimate is only approximate, and the exact load current threshold, to trigger PFM, can vary greatly with input and output voltage. The Typical Performance Characteristics shows mode change thresholds for several typical operating points. When the regulator detects this threshold, the reference voltage is increased by approximately 10mV. This causes the output voltage to rise to meet the new regulation point. When this point is reached, the converter stops switching and much of the internal circuitry is shut off, while the reference is returned to the PWM value. This saves supply current while the output voltage naturally starts to fall under the influence of the load current. When the output voltage reaches the PWM regulation point, switching is again started and the reference voltage is again increased by about 10mV; thus starting the next cycle. Typical waveforms are shown in Figure 24

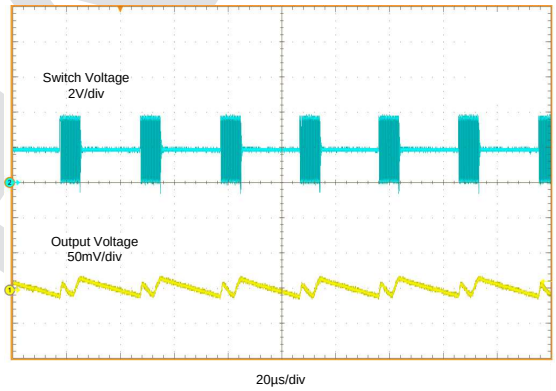

Figure 24. Typical PFM Mode Waveforms: V_{IN}=3.6V, V_{OUT}=1.8V, I_{OUT}=10mA

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The actual output voltage ripple will depend on the feedback divider ratio and on the delay in the PFM comparator. The frequency of the PFM "bursts" will depend on the input voltage, output voltage, load and output capacitor. Within each "burst" the device switches at 3.0 MHz (typ.). If the load current increases above the threshold, normal PWM operation is resumed. This mode provides high light load efficiency by reducing the amount of supply current required to regulate the output at small load currents.

Because of normal part-to-part variation, the LMZ20502 may not switch into PFM mode at high input voltages. This is may be seen with output voltages of about 1.2V and below, at input voltages of about 4.2V and above.

Internal Synchronous Rectifier

The LMZ20502 uses an internal NMOS FET as a synchronous rectifier to minimize switch voltage drop and increase efficiency. The NMOS is designed to conduct through its body diode during switch dead time. This dead time is imposed to prevent supply current "shoot-through".

Current Limit Protection

The LMZ20502 incorporates cycle-by-cycle peak current limit on both the high and low side MOSFETs. This feature limits the output current in case the output is overloaded. During the overload, the peak inductor current is limited to that value found in the Electrical Characteristics table under the heading of "I_{LIM}".

In addition to current limit, a short circuit protection mode is also implemented. When the feedback voltage is brought down to less than 300mV, but greater than 150mV, by a short circuit, the synchronous rectifier is turned off. This provides more voltage across the inductor to help maintain the required volt-second balance. If a "harder" short brings the feedback voltage to below 150mV, the current limit and switching frequency are both reduced to about ½ of the nominal values. In addition, when the current limit is tripped, the device stops switching for about 85µs. At the end of the time-out, switching resumes and the cycle repeats until the short is removed.

The effect of both overload and short circuit protection can be seen in Figure 25. This graph demonstrates that the device will supply slightly more than 2A to the load when in overload and much less current during fold-back mode. This is typical behavior for any regulator with this type of current limit protection.

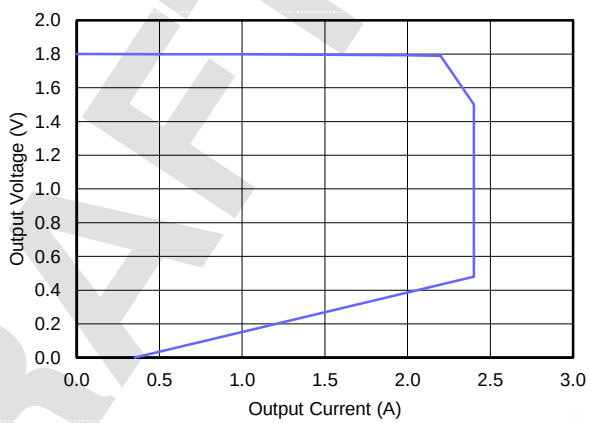

Figure 25. Typical Current Limit Profile, V_{IN} = 5V, V_{OUT} = 1.8V

Start-up

Start-up and shutdown of the LMZ20502 is controlled by the EN input. The thresholds on this input are found in the Electrical Characteristics table. A valid input voltage must be present on VIN before the enable control is asserted. The maximum voltage on the EN pin is 5.5V or VIN, whichever is smaller.

The LMZ20502 features a current limit based soft-start, that prevents large inrush currents and output overshoots as the regulator is starting up. The peak inductor current is stepped-up in a staircase fashion during the soft start period. A typical start-up event is shown in Figure 26

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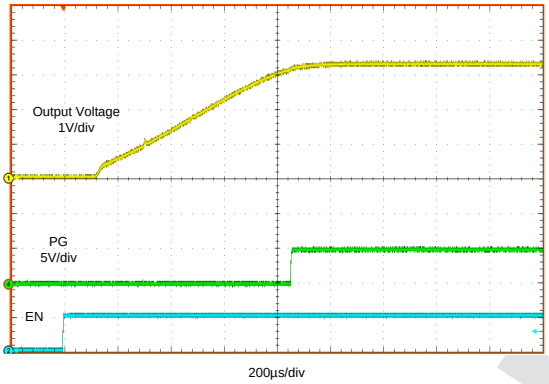

Figure 26. Typical Start-up Waveforms, V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A

Drop-out Behavior

When the input voltage is close to the output voltage the regulator will operate at very large duty cycles. Normal time delays of the internal circuits prevents the attainment of controlled duty cycles near 100%. In this condition the LMZ20502 will skip switching cycles in order to maintain regulation with the highest possible input to output ratio. Some increase in output voltage ripple may appear as the regulator skips cycles. As the input voltage gets closer to the output voltage, the regulator will eventually reach 100% duty cycle, with the high side switch turned on. The output will then follow the input voltage minus the drop across the high side switch and inductor resistance. Figure 27 and Figure 28 show typical drop-out behavior for output voltages of 2.5V and 3.3V.

Since the LMZ20502 has no internal regulator, the R_{dson} of the power FETs will increase at low input voltages. This will result in degraded efficiency at output currents of greater than 1A and input voltages below about 2.9V. Also, this combination of operating point tends to increase the effective duty cycle which may result in increased output voltage ripple.

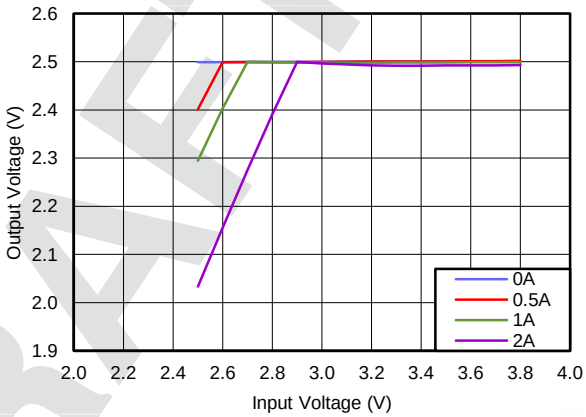

Figure 27. Typical Drop-out Behavior, V_{OUT} = 2.5V

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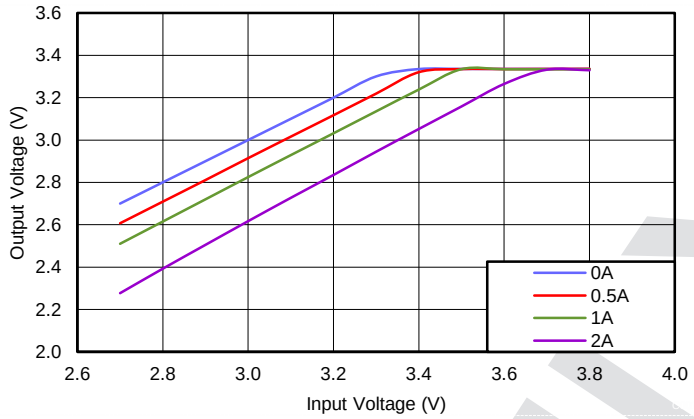

Figure 28. Typical Drop-out Behavior, V_{OUT} = 3.3V

Power Good Flag Function

The operation of the power good flag function is described in the diagram shown in Figure 29

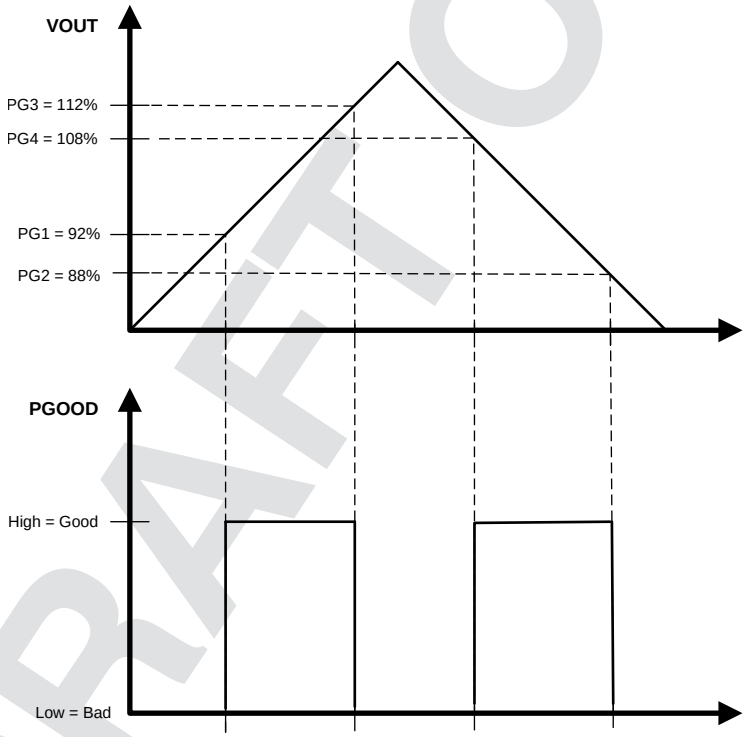

Figure 29. Typical Power Good Flag Operation

When used, the power good flag should be connected to a logic supply through a pull-up resistor. It can also be pulled-up to either V_{IN} or V_{OUT}, through an appropriate resistor, as desired. If this function is not needed, the PG output should be left floating. The current through this flag pin should be limited to less than 4mA. A pull-up resistor of ≥1.5kΩ will satisfy this requirement. When the EN input is pulled low, the PG flag output will also be forced low, assuming a valid input voltage is present.

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Application Information

SETTING THE OUTPUT VOLTAGE

The LMZ20502 regulates its feedback voltage to 0.6V (typ). A feedback divider, shown in the Typical Application Circuit, is used to set the desired output voltage. Equation 1 can be used to select R_{FBB} .

$$R_{FBB} = \frac{0.6}{(V_{out} - 0.6)} \cdot R_{FBT} \tag{1}$$

For best results, R_{FBT} should be chosen between 30kΩ and 300kΩ. See Table 3 for recommended values for typical output voltages.

CAPACITOR SELECTION

Output and Feed-forward Capacitors

The LMZ20502 is designed to work with low ESR ceramic capacitors. The **effective** value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have large voltage coefficients, in addition to normal tolerances and temperature coefficients. Under D.C. bias, the capacitance value drops considerably. Larger case sizes and/or higher voltage capacitors are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum **effective** capacitance up to the desired value. This can also ease the RMS current requirements on a single capacitor. Typically, 10V, X5R, 0805 capacitors are adequate for the output, while 16V caps may be used on the input. Some recommended component values are provided in Table 3. Also, shown are the measured values of **effective** input and output capacitance for the given capacitor. If smaller values of output capacitance are used, C_{FF} must be adjusted to give good phase margin. In any case, load transient response will be compromised with lower values of output capacitance. Values much lower than those found in Table 3 should be avoided. In practice, the output capacitor and C_{FF}, are adjusted for the best transient response and highest loop phase margin. Load transient testing and Bode plots are the best way to validate any given design. Application report SNVA364A, found here, http://www.ti.com/lit/an/snva364a/snva364a.pdf details a simple method of creating a Bode plot with basic laboratory equipment. A careful study of the temperature and bias voltage variation of the target capacitor should be made in order to ensure that the minimum values of **effective** capacitance are provided. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH ® tool: http://www.ti.com/lsds/ti/analog/webench/overview.page.

The maximum value of total output capacitance should be limited to between 100µF and 200µF. Large values of output capacitance can prevent the regulator from starting-up correctly and adversely affect the loop stability. If values in the range given above, or larger, are to be used, then a careful study of start-up at full load and loop stability must be performed.

Input Capacitors

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. An **effective** value of at least 14µF is normally sufficient for the input capacitor. If the main input capacitor(s) can not be placed close to the module, then a small 10nF to 100nF capacitor should be placed directly at the module, across the supply and ground pins.

Many times it is desirable to use an electrolytic capacitor on the input, in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by long power leads. This method can also help to reduce voltage spikes that may exceed the maximum input voltage rating of the LMZ20502. The use of this additional capacitor will also help with voltage dips caused by input supplies with unusually high impedance.

Most of the switching current passes through the input ceramic capacitor(s). The approximate, worst case, RMS value of this current can be calculated with Equation 2 and should be checked against the manufactures maximum ratings.

$$I_{RMS} \approx \frac{I_{out}}{2} \tag{2}$$

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Table 3. RECOMMENDED COMPONENT VALUES

VOUT	R_{FBB}	R_{FBT}	COUT	EFFECTIVE COUT(1)	C_{FF}	CIN	EFFECTIVE CIN(1)
0.8V	121 kΩ	40.2 kΩ	2x 10µF	18 µF	39 pF	2x 10µF	14 µF
1.2V	30.1 kΩ	30.1 kΩ	10 µF	8.8 µF	20 pF	2x 10µF	14 µF
1.8V	40.2 kΩ	80.6 kΩ	10 µF	8.4 µF	16 pF	2x 10µF	14 µF
2.5V	47.5 kΩ	150 kΩ	10 µF	7.8 µF	12 pF	2x 10µF	14 µF
3.3V	53.2 kΩ	237 kΩ	10 µF	7.1 µF	82 pF	2x 10µF	14 µF
3.6V	53.2 kΩ	267 kΩ	10 µF	6.8 µF	82 pF	2x 10µF	14 µF

(1) CIN = COUT = 10µF, 16V, 0805, X7R, Samsung CL21B106KOQNNNE. COUT measured at V_{OUT}; CIN measured at 3.3V.

MAXIMUM AMBIENT TEMPERATURE

As with any power conversion device, the LMZ20502 will dissipate internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter, above ambient. The internal die temperature is a function of the ambient temperature, the power loss and the effective thermal resistance (θ_{JA}) of the device and PCB combination. The maximum internal die temperature for the LMZ20502 is 125°C; thus establishing a limit on the maximum device power dissipation and therefore load current at high ambient temperatures. Equation 3 shows the relationships between the important parameters.

$$I_{out} = \frac{(T_J - T_A)}{\theta_{JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{out}} \tag{3}$$

It is easy to see that larger ambient temperatures and larger values of θ_{JA} will reduce the maximum available output current. The effective θ_{JA} is a critical parameter and depends on many factors such as power dissipation, air temperature, PCB area, copper heatsink area, air flow, and adjacent component placement. The resources found in Table 4 can be used as a guide to estimate the θ_{JA} for a given application environment. The efficiency found in the equation, η, should be taken at the elevated ambient temperature. For the LMZ20502 the efficiency is about two to three percent lower at high temperatures. Therefore, a slightly lower value than the typical efficiency can be used in the calculation. In this way Equation 3 can be used to estimate the maximum output current for a given ambient, or to estimate the maximum ambient for a given load current.

Table 4. RESOURCES FOR ESTIMATING θ_{JA}

Title	Link
SNVA419B	http://www.ti.com/lit/an/snva419c/snva419c.pdf
SNVA424	http://www.ti.com/lit/an/snva424a/snva424a.pdf
SNVA183B	http://www.ti.com/lit/an/snva183b/snva183b.pdf
SNOA401R	http://www.ti.com/lit/an/snoa401r/snoa401r.pdf

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A typical curve of maximum load current vs. ambient temperature is shown in Figure 30. This graph assumes a θ_{JA} of 44°C/W and an input voltage of 5V. A θ_{JA} of 44°C/W is the approximate value for the LMZ20502 evaluation board.

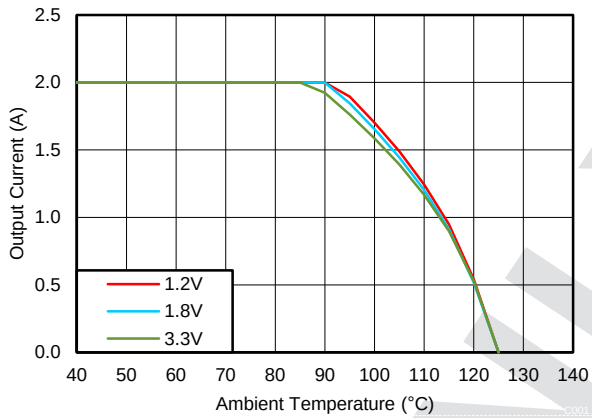

Figure 30. Maximum Output Current vs. Ambient Temperature, θ_{JA} = 44°C/W, Vin = 5V

PCB LAYOUT GUIDELINES

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor and the module ground, as shown in Figure 31. This loop carries fast transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages will disrupt the proper operation of the converter. Because of this, the traces in this loop should be wide and short, and the loop area as small as possible to reduce the parasitic inductance. Figure 32 shows a recommended layout for the critical components of the LMZ20502; the top side metal is shown in red. This PCB layout is a good guide for any specific application. The following important guidelines should also be followed:

1. **Place the input capacitor CIN as close as possible to the VIN and GND terminals.** VIN (pin 8) and GND (pin 6) are on the same side of the module, simplifying the input capacitor placement.
2. **Place the feedback divider as close as possible to the FB pin on the module.** The divider and C_{FF} should be close to the module, while the length of the trace from VOUT to the divider can be somewhat longer. However, this latter trace should not be routed near any noise sources that can capacitively couple to the FB input.
3. **Connect the EP pad to the GND plane.** This pad acts as a heat-sink connection and a ground connection for the module. It must be solidly connected to a ground plane. The integrity of this connection has a direct bearing on the effective θ_{JA}.
4. **Provide enough PCB area for proper heat-sinking.** As stated in the MAXIMUM AMBIENT TEMPERATURE section, enough copper area must be used to provide a low θ_{JA}, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers should be made with two ounce copper; and no less than one ounce.
5. **The resources in Table 5 provide additional important guidelines**

Table 5. PCB LAYOUT RESOURCES

Title	Link
SNVA021C	http://www.ti.com/lit/an/snva021c/snva021c.pdf
SNVA054C	http://www.ti.com/lit/an/snva054c/snva054c.pdf
SLUP230	http://www.ti.com/lit/ml/slup230/slup230.pdf

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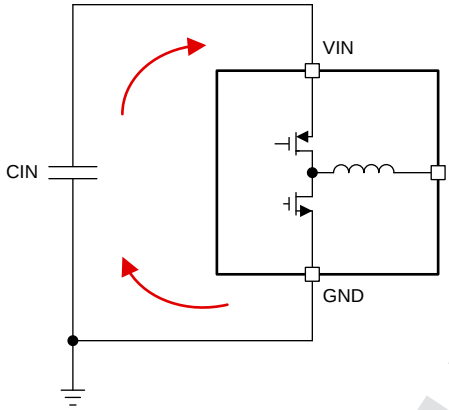

Figure 31. Current Loops with Fast Transient Currents

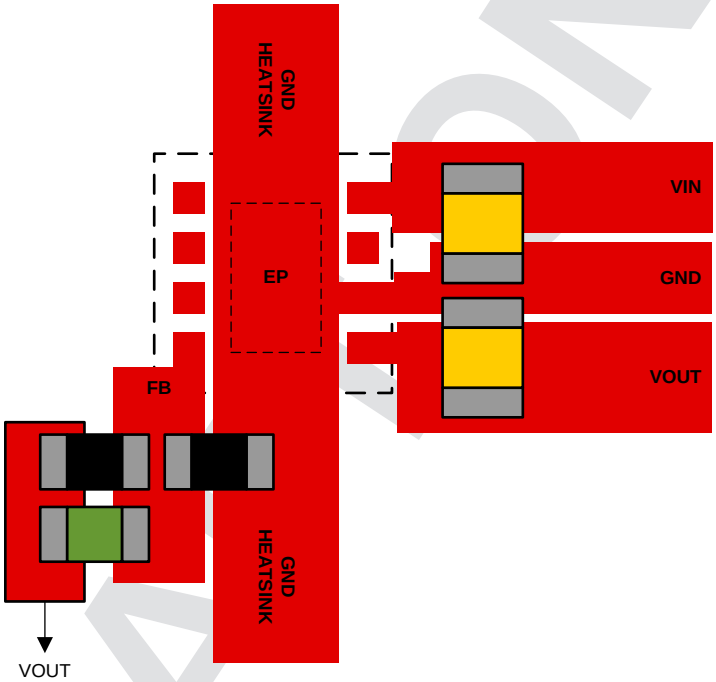

Figure 32. Example PCB Layout

SOLDERING INFORMATION

Proper operation of the LMZ20502 requires that it be correctly soldered to the PCB. This is especially true regarding the EP. This pad acts as a quiet ground reference for the device and a heatsink connection. Use the following recommendations when utilizing machine placement of the device:

- Dimension of area for pick-up: 2mm x 2.5mm.
- Use a nozzle size of less than 1.3mm in diameter, so that the head does not touch the outer area of the package.
- Use a soft tip pick and place head.
- Add 0.05mm to the component thickness so that the device will be released 0.05mm into the solder paste without putting pressure or splashing the solder paste.
- Slow the pick arm when picking the part from the tape and reel carrier and when depositing the device on the board.
- If the machine releases the component by force, use the minimum force and no more than 3N.

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- For PCBs with surface mount components on both sides, it is suggested to put the LMZ20502 on the top side. In case the applications requires bottom side placement, a reflow fixture may be required to protect the module during the second reflow.

In addition, please follow the important guidelines found in: http://www.ti.com/lit/an/snoa401r/snoa401r.pdf. The curves in Figure 33 and Figure 34 show typical soldering temperature profiles.

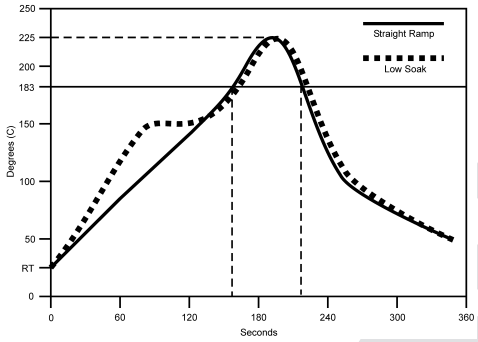

Figure 33. Typical Reflow Profile Eutectic (63Sn/37Pb) Solder Paste

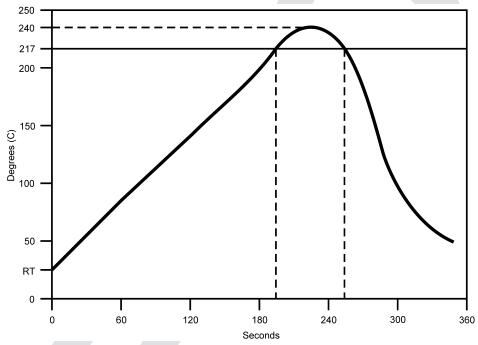

Figure 34. Typical Reflow Profile Lead-Free (SCA305 or SAC405) Solder Paste

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